



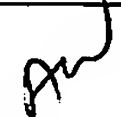
UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,372	02/25/2002	Michael E. Connell	2269-5083US	1935
24247	7590	05/10/2004	EXAMINER	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			ROMAN, ANGEL	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 05/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/082,372		CONNELL ET AL.	
	Examiner		Art Unit	
	Angel Roman		2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-86 is/are pending in the application.
- 4a) Of the above claim(s) 8-10, 17-22, 25-27, 29, 40-42, 49-54, 61, and 72-86 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 11-16, 23, 24, 30-39, 43-48, 55-58 and 62-71 is/are rejected.
- 7) ☒ Claim(s) 28, 59 and 60 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>02252002</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Specie I, figure 10 in Paper No. 01162004 is acknowledged. Applicants indicated claims 1-7, 9-28, 30-60 and 62-74 are representative of specie I, figure 10, however claims 8-10, 17-22, 25-27, 29, 34-36, 40-42, 49-54, 61 and 72-74 do not represent the elected specie I, since these claims describe patentable distinct species and are therefore not being considered by the examiner.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6, 7, 11, 15, 16, 23, 24, 33-36, 38, 39, 43, 47, 48, 55-57, 65, 66, 70 and 71 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al. U.S. Patent 3,861,969 A.

Ono et al. discloses a method for producing a non-warped semiconductor die from a wafer 41 having a front side, a back side, and a front side layer 42 on a portion of said wafer 41 causing a stress (see figure 4b), said method comprising; reducing a cross section of said semiconductor die by thinning said semiconductor die; applying a rigid stress balancing layer 46 to said wafer 41 (see figure 4f); and singulating said wafer into a plurality of semiconductor dies (see column 5, lines 57-58).

The front side layer 42 comprises a layer of passivation material applied in fabrication of said semiconductor die.

The thinning comprises grinding the back surface (see column 5, lines 6-8).

The semiconductor die comprises an integrated circuit semiconductor die.

The stress-balancing layer 46 substantially covers the wafer's backside (see figure 4h).

The stress-balancing layer 46 comprises a film.

The stress-balancing layer (SBL) comprises an alloy (see column 5, lines 8-13).

The semiconductor die may comprise one of a DIP, SIP, ZIP, PLCC, SOJ, SIMM, DIMM, LOC, QFP, SOP, TSOP, and a flip-chip.

The SBL comprises a metal alloy such as Au-Ge, Sn, or Au-Sn, which are materials that can be marked with indicia or optical radiation energy.

4. Claims 1, 30, 33, 62 and 65 are rejected under 35 U.S.C. 102(e) as being anticipated by Okuno et al. U.S. Patent 6,579,748 B1.

Okuno discloses a method for producing a non-warped semiconductor dice having a die front side, a die back side, and a stress applied thereto by a die front side layer, said method comprising; forming a semiconductor wafer 10 having a front side, a back side, a plurality of micro-circuits on said front side, and a front side layer applying stress to said wafer (conventional layer form during electronic circuit fabrication, e.g. intermetallic dielectric layer or layer 18); reducing a cross sectional area of said wafer by thinning said back side (see figure 25); singulating said wafer into a plurality of semiconductor dice (see figure 27); and applying a rigid stress-balancing layer to said thinned back side under conditions which apply a back side stress generally equivalent to said front side stress upon restoration to conditions of said semiconductor die use (see column 9, lines 5-15). The stress-balancing layer has a coefficient of thermal expansion substantially similar to that of said front side layer (see column 10, lines 45-55).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

Art Unit: 2812

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 5, 12, 13, 14, 31, 32, 37, 44-46, 63, 64 and 67-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono et al. U.S. Patent 3,861,969 A.

Ono et al. is applied as above but lacks anticipation on disclosing a chemical mechanical method for thinning the wafer; applying the SBL by chemical vapor deposition or VPE processes; applying a die attached adhesive to the SBL; and applying a temporary reinforcement layer over the wafer front side prior to thinning the back side.

With respect to disclosing a chemical mechanical method for thinning the wafer, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use a chemical mechanical polishing process to thinned the

Art Unit: 2812

wafer in the primary reference of Ono et al. since the chemicals would ease the material removing process on the wafer.

Regarding applying the SBL by chemical vapor deposition (CVD) or VPE processes. CVD and VPE are widely used deposition methods for depositing metal layers, therefore it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use them to deposit the metal SBL layer in the primary reference of Ono et al. in order to optimize the metal layer.

As to applying a die attached adhesive to the SBL, it would have been obvious to one having ordinary skills in the art at the time the invention was made to apply a die attach adhesive to the SBL in the primary reference of Ono in order to secure the finished device to a package substrate.

Regarding applying a temporary reinforcement layer over the wafer front side prior to thinning the back side, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to apply a temporary reinforcement layer over the wafer front side since it would prevent damage to the wafer during the thinning process.

9. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno et al. U.S. Patent 6,579,748 B1.

Okuno et al. is applied as above but lacks anticipation on using polytetrafluoroethylene tape as the SBL. Selecting polytetrafluoroethylene tape as the SBL material in the primary reference of Okuno et al. is only considered to be the use of

Art Unit: 2812

a " preferred " or " optimum " material out of a plurality of well known materials that a person having ordinary skill in the art at the time the invention was made would have find obvious to provide using routine experimentation.

Allowable Subject Matter

10. Claims 28, 59, 60 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record either in single or in combination failed to anticipate or render obvious the limitations of exposing a tape applied to the SBL with a laser as required by claims 28, 59 and 60.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sakai et al., Liu, Wakabayashi et al., Unno et al., Mikata et al. and Jang disclosed methods for producing non-warped semiconductor dice by applying a layer to a second side of a wafer.


Art Unit: 2812

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
May 3, 2004


John F. Niebling
Supervisory Patent Examiner
Technology Center 2800